
Generic CPU Board #1 Users Manual

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This document contains technical information needed to use and configure the Generic CPU Board (GCB). All connectors and configuration jumpers are identified (physical location/device id.) and logically defined. Programming information regarding address space layout etc. is also supplied herein.

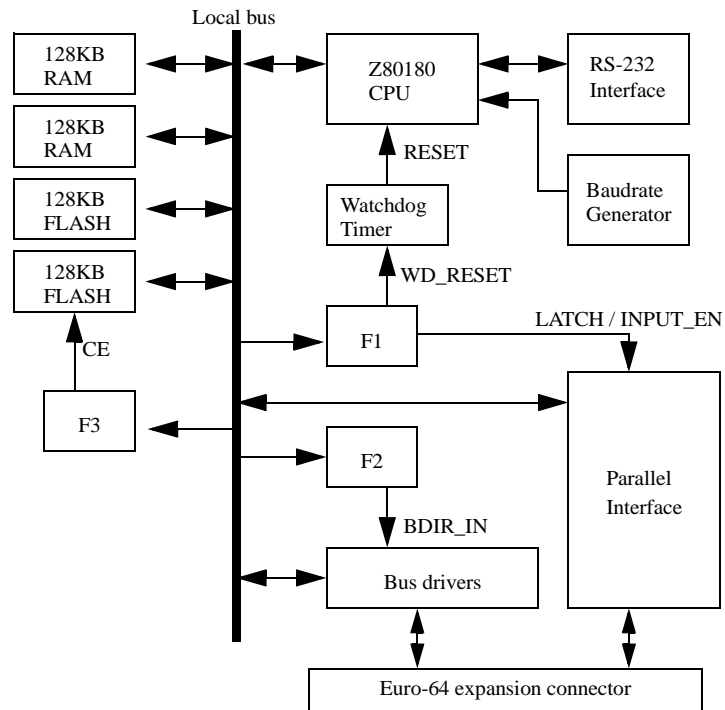
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1.0 Functional description

1.1 Overview

The Generic CPU Board (GCB) is a building block for modular embedded systems. It is based on the Zilog Z80180/Z8S180 CPU which is available with 10, 20 or 33 MHz clock frequency. A fully equipped GCB contains the following:

- Z80180 CPU with built-in DMA, UART, timers and MMU
- 256KB FLASH PROM and 256KB SRAM
- Two full duplex RS-232 channels
- One TTL level 8 bit parallel input port and one latched 8 bit output port
- Watchdog timer with power-on reset and brown-out protection
- Standard Europa format PCB 100 x 160 mm with 64 pin Euro connector type C
- Fully buffered address, data and control signals available on Euro connector, allows easy expansion of memory (512KB max) and I/O ports (128 max) on external boards.



Picture 1.

CPU board logical block diagram.

1.2 Address space layout

The address space is sub-divided into GCB local space and external space. At most 1MB memory and 256 I/O ports can be accessed directly by the Z80180 CPU. The lower half of memory and I/O address spaces are defined to be GCB local. All CPU bus cycles are visible at the 64 pin Euro connector. Memory and I/O address spaces are described in the table below.

I/O address [hex]	Description
40	Local 8 bit parallel input port
50	Watchdog reset, write-only
60	Local 8 bit latched parallel output port
80-FF	External ports, accessed through Euro-64 connector

Table 1. *I/O address space layout.*

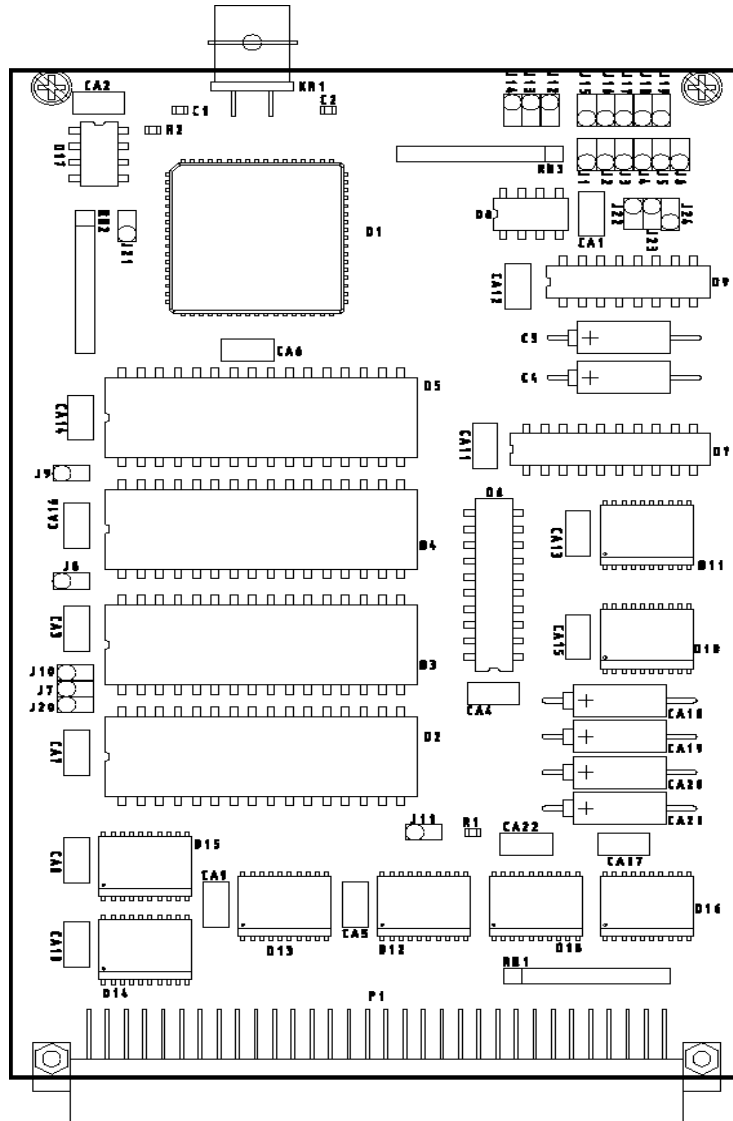
Memory address [hex]	Description
00000-000FF	Local FLASH PROM 1, device D3, boot block
00100-1FFFF	Local RAM 1
20000-3FFFF	Local RAM 2
40000-5FFFF	Local FLASH PROM 1, device D3
60000-7FFFF	Local FLASH PROM 2, device D2
80000-FFFFFF	External memory, accessed through Euro-64 connector

Table 2. *Memory address space layout.*

2.0 Board configuration and connectors

2.1 Circuit board disposition

Below is a top view of the GCB printed circuit board, showing component identifiers and placement.



2.2 Jumpers and connectors

2.2.1 Modem signals and synchronous half duplex serial port I/O connector.

Item	Pin	Description
J1	1	/RTS0
	2	GND
J2	1	/CTS0
	2	GND
J3	1	/DCD0
	2	GND
J4	1	TXS
	2	GND
J5	1	RXS
	2	GND
J6	1	CKS
	2	GND

Table 3. *Jumper J1-J6 signal descriptions.*

2.2.2 RS-232 serial port bit rate selection.

ASCI clock = EXO3_f0 / pow2(1+N), N = b0 + 2 * b1 + 4 * b2.

Item	Pin	Description
J12	1	GND
	2	ASCI clock select b0
J13	1	GND
	2	ASCI clock select b1
J14	1	GND
	2	ASCI clock select b2

Table 4. *Jumper J12-J14 signal descriptions.*

2.2.3 Serial port to RS-232 converter signal path break-and-insert points.

Item	Pin	Description
J15	1	TXA1 from CPU (output)
	2	TXA1 to RS-232 converter (input)
J16	1	TXA0 from CPU (output)
	2	TXA0 to RS-232 converter (input)
J17	1	RXA1 to CPU (input)
	2	RXA1 from RS-232 converter (output)
J18	1	RXA0 to CPU (input)
	2	RXA0 from RS-232 converter (output)
J19	1	GND
	2	GND

Table 5. *Jumper J15-J19 signal descriptions.*

2.2.4 RS-232 I/O connector, channel 0 & 1.

Item	Pin	Description
J22	1	TXA1 (RS-232 output)
	2	TXA0 (RS-232 output)
J23	1	RXA1 (RS-232 input)
	2	RXA0 (RS-232 input)
J24	1	GND
	2	GND

Table 6. *Jumper J22-J24 signal descriptions.*

2.2.5 Miscellaneous configuration jumpers.

Item	Pin	Description
J7	1	FLASH PROM 2 /WE (input)
	2	/WR from CPU (output)
J8	1	FLASH PROM 1 NC (input)
	2	+5V
J9	1	FLASH PROM 1 /WE (input)
	2	/WR from CPU (output)
J10	1	+5V
	2	FLASH PROM 1 NC (input)
J11	1	GND
	2	74xx574 latch /OE
J20	1	FLASH PROM 2 NC (input)
	2	+5V
J21	1	WD_RESET (output)
	2	MAX 690 watchdog input

Table 7.*Jumper J7-J11, J20-J21 signal descriptions.*

2.3 Euro-64 expansion connector

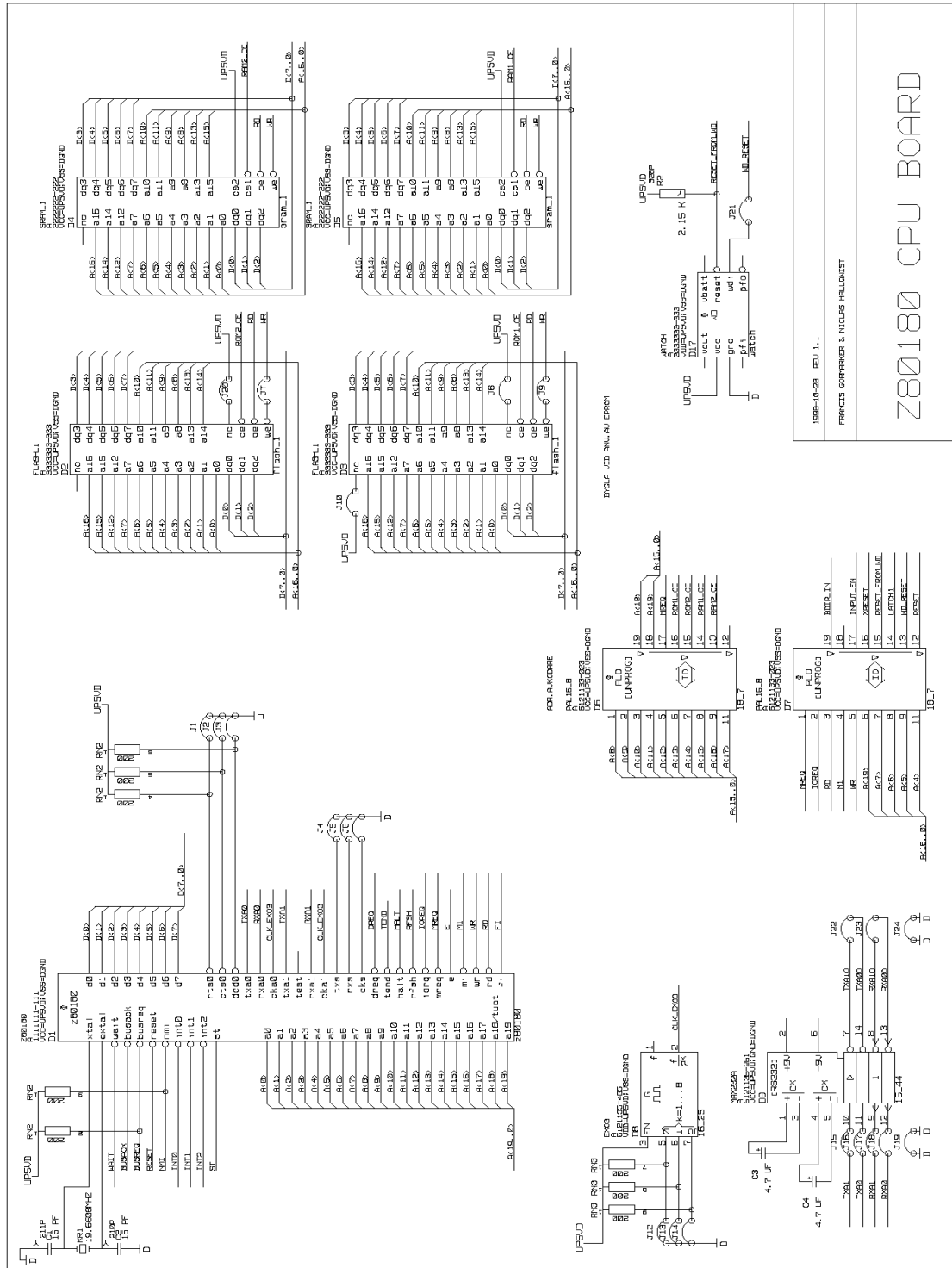
Signal	A		C	Signal	
GND	1		33	GND	
/BIORQ	2		34	/XRESET *	* System reset input
/BMREQ	3		35	/BINT0	
/BRD	4		36	/BINT1	
/BWR	5		37	/BINT2	
/BRESET *	6		38	/BWAIT	* System reset output
BCLK	7		39	/BDREQ	
/BM1	8		40		
	9		41		
BD_IN0	10		42	BD_IN1	BD_IN0-7: local input port
BD_IN2	11		43	BD_IN3	
BD_IN4	12		44	BD_IN5	
BD_IN6	13		45	BD_IN7	
BD_OUT0	14		46	BD_OUT1	BD_OUT0-7: local output port
BD_OUT2	15		47	BD_OUT3	
BD_OUT4	16		48	BD_OUT5	
BD_OUT6	17		49	BD_OUT7	
BD0	18		50	BD1	
BD2	19		51	BD3	
BD4	20		52	BD5	
BD6	21		53	BD7	
BA0	22		54	BA1	
BA2	23		55	BA3	
BA4	24		56	BA5	
BA6	25		57	BA7	
BA8	26		58	BA9	
BA10	27		59	BA11	
BA12	28		60	BA13	
BA14	29		61	BA15	
BA16	30		62	BA17	
BA18	31		63	BA19	
+5V	32		64	+5V	

Tabell 8.

Signal overview, Euro-64 expansion connector.

3.0 Detailed design description

3.1 Complete circuit drawing, sheet 1



3.2 Complete circuit drawing, sheet 2

